ABSTRACT OF THE DISCLOSURE

In one aspect, the present invention is directed to a technique of, and circuitry and system for enhancing the performance of data communication systems using receiver based decision feedback equalization circuitry. In one embodiment, the equalization circuitry and technique employs a plurality of data slicers (for example, two) to receive an analog input and output a binary value based on the reference or slicer level. The output of the data slicers is provided to logic circuitry to determine whether the analog input was a binary high or binary low. In those instances where the data slicers "agree" and both indicate either a high or a low, the logic circuitry outputs the corresponding binary value. In those instances where the data slicer do not "agree" – that is, where one data slicer indicates the input to be a binary or logic high value and the other data slicer indicates the input to be a binary or logic low value, in one embodiment, the logic circuitry outputs the complement of the previous binary value. In another embodiment, the logic circuitry selects the output from the slicer that changed its output from the previous binary value. In yet another embodiment where the slicers do not "agree", the logic circuitry selects the decision of the data slicer with higher slicer value if the previous binary value was "high", or selects the decision of the data slicer with the lower slicer value if the previous binary value was "low". The data slicers employ slicer levels that may be fixed, pre-programmed, predetermined, preset, changed, modified, optimized, enhanced and/or programmed or re-programmed (for example, adaptively) before or during operation of the decision feedback equalization circuitry.